REMARKS

Acknowledgment of receipt and acceptance of the replacement drawing sheet filed February 1, 2008, is noted with appreciation.

Claims 6 to 12 were objected to and, in particular, the Examiner suggested amendments to claims 6, 8 and 10 for consistency and clarification. The Examiner's suggestion as to claim 10 has been adopted by this amendment; however, a slight variation of the Examiner's suggestions as to claims 6 and 8 has been adopted by this amendment. Specifically, the language now used is "a plurality of said multiple subcomponents", this being more accurate of the disclosed invention. As amended, it is requested that the objection to claims 6 to 12 be withdrawn.

The specification was objected to as failing to provide proper antecedent basis for the claimed subject matter of claim 1. Claim 1 recites that "each subcomponent [of the first processing unit] being designed to process the time-synchronous multi-media data in a specific and different way" and "each subcomponent [of the second processing unit] being designed to process the time-synchronous multi-media data in a specific and different way". While acknowledging that the specification specifically describes the subcomponents CODEC 6a, FILTER 6b and PACKETIZER 6c of the first processing unit 3 (shown in Figure 3 of the drawings), the Examiner has confused the subcomponents of the second processing unit with those shown in Figure 1 of the drawings. As shown in Figure 3 of the drawings, the subcomponents of the second processing unit 4 are the CODEC 7a, FILTER 7b and PACKETIZER 7c. Moreover, these are only examples of the types of subcomponents, each of which "process the time-synchronous multi-media data in a specific and different way"; i.e., a CODEC processes data in a specific way and that way is different from the way a FILTER processes data in its specific way, etc. It will be noted that as described on page12, lines 24–27, and illustrated in Figure 3, there may be other subcomponents for further processing and transmission of frames, including for example a memory buffer as a memory buffer or similar components, as described for example on page 8,

lines 23–27, of the specification. It is therefore clear, that there is proper antecedent basis in the specification for the language of claim 1, and withdrawal of the objection to the specification is therefore respectfully requested.

Claims 1 to 18 are pending in the application. Claims 6, 8 and 10 have been amended as described above. In addition claims 1 has been amended to make clear the environment in which the invention is practiced and the types of subcomponents used in the practice of the invention. Claims 6, 8, 17, and 18 have been amended to reflect the amendments to claim 1. These amendments are made in an effort to expedite the prosecution of the application.

Claims 13 and 14 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. This rejection is respectfully traversed for the reason that the Examiner has misconstrued the disclosure and fails to recognize what the level of skill in the art is. As to the latter point, the Examiner on page 27 of the Office Action correctly recognizes that Koichi Funaya who provided the declaration under 37 C.F.R. 1.132 filed with the last amendment is, by reason of his education and experience, an expert in the art; however, the Examiner fails to understand the probative nature of expert opinion evidence. In our American jurisprudence system, and under the Federal Rules of Evidence (which is controlling in the U.S. Patent and Trademark Office), the opinions of lay witnesses (i.e., the Examiner's "routineer") is strictly limited when it comes to scientific, technical or other specialized knowledge (Rule 701, Federal Rules of Evidence). In other words, the opinion of a "routineer" would not be probative on the question of enablement. But to suggest, as the Examiner has, that Mr. Funaya is not competent to know what the level of skill in the art would be for one of ordinary skill in the art to which the disclosed invention is related is patently absurd. In paragraph 3 of his declaration under 37 C.F.R. 1.132, Mr. Funaya describes the level of skill of one of ordinary skill in the art to which the disclosed invention is related, that being the Statutory standard. The role of expert opinion is set out in Rules 702 to 706 of the Federal Rules of Evidence. For the Examiner's reference, copies of the relevant pages of the Federal

Rules of Evidence are attached. Concerning the Examiner's remarks in the second full paragraph on page 7 of the Office Action, Applicants have not admitted that the specification fails to support and enabling disclosure for the claimed invention. Moreover, arguments of counsel have not been submitted in evidence; rather, that is the purpose of Mr. Funaya's declaration. The Examiner is respectfully requested to re-read Mr. Funaya's declaration and to withdraw this ground of rejection.

Claims 1 to 4 and 6 to 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over International Patent Publication WO 00/62254 of Zahn in view of U.S. Patent No. 6,694,373 to Sastry et al. This rejection is again respectfully traversed for the reason that the combination of Zahn and Sastry et al. neither discloses nor suggests the claimed invention.

The disclosed and claimed invention is directed to an apparatus for the processing and transmission of an "apparatus for the transmission of time-synchronous multi-media data from a sender to a receiver using an IP (Internet Protocol) network", and in particular, the network contemplated by the inventors is the Internet where the time-synchronous multi-media data is packetized for transmission using the Internet Protocol (IP). Claim 1, as amended, makes this perfectly clear.

The Examiner continues to contend that "Zahn discloses an apparatus (see FIG.1, 2; apparatus 1) for the transmission of time-synchronous data (see FIG. 3, video signal 50; see page 4, paragraph 3–8; see page 9, last paragraph; real time/synchronous video signal utilizing MPEG or HDTV) from a sender to a receiver using a network (see page 4–6; a video signal must transmit from a transmitter to a receiver/customer over a network), wherein the data is processed and transmitted at the sender as well as the receiver (see FIG. 1, 2, 4, 5, the video data is processed at transmitter or receiver/customer; see page 9, last paragraph) . . ." On page 9 of Zahn, the apparatus 1 is described as being connected by a PCI bus 2 to a CPU of a personal computer. For the Examiner's benefit, PCI stands for Peripheral Component Interconnect, a bus standard designed by Intel for personal computers. See page 537,

second definition, of *Newton's Telecom Dictionary*, 14th Ed. (1998), copy of which was previously submitted. In other words, the apparatus 1 is a processor board which is inserted into a PCI bus card slot inside a personal computer. Zahn describes Figure 3 as illustrating "temporally sequential data packets like those occurring in video processing". This is not the same thing as time-synchronous data. As described at the top of page 11 of Zahn, "video signal 50 has temporally discrete and sequential data packets, so-called frames 100. . . which have the constant temporal spacing T, . . ." Zahn goes on to describe that a first frame 101 is requested by the dispatcher program of the primary processor along the PCI bus 2 along the local bus 7 of the apparatus 1. This data packet 101 is then decompressed by the decoder 3. This data is clearly not time-synchronous. The data packets are temporarily sequential; that is, they following one another in a sequential order, but they are static (i.e., stored on hard disk) until requested by the dispatcher program. The last paragraph of page 9 of Zahn describes the internal components of the PCI card apparatus 1. The acronyms "MPEG" and "HDTV" respectively stand for Motion Picture Experts Group and High Definition Television (see pages 341 and 465, *Newton's Telecom Dictionary* by Harry Newton (1998), copies attached). MPEG is a video encoding scheme, and HDTV merely describes a type of television having a 16-to-9 aspect ratio and a prescribed pixel resolution. Non-linear video editors of the type Zahn describes implement MPEG video encoding on video frames that have resolutions meeting the HDTV definition.

Thus, contrary to the Examiner's contention, Zahn does not disclose transmission of time-synchronous data and certainly does not disclose transmission of that data using a network of any type. On the contrary, Zahn discloses a video processor board for a personal computer (PC) for connection to the Peripheral Component Interconnect (PCI) bus. This video processor board is for non-linear video editing (NLE, see page 4, line 8, of Zahn) systems which, by their very nature, are not transmitting time-synchronous data from a sender to a receiver. The Zahn video processor board may include multiple processors, but their operation is entirely different from the claimed first and second processors. In the case of the Zahn video

processor board, the multiple processors are for the purpose of improving rendering speed of the video data being edited. This process is not real time. In contrast, the first and second processing units of the claimed invention operate in a manner to avoid time delays and resulting dropping of frames in the transmission of the time-synchronous data. This is process is real time.

Further explanations of HDTV, NLE systems and video processing expansion cards were previously provided in articles from Wikipedia. At the heart of any NLE system is a video capture card which is inserted into an option card slot (currently a PCI or PCI express slot) in a PC. Previously submitted was a copy of a paper entitled "Video 101" from ATI corporation, now merged with AMD corporation, which describes the fundamentals. Also attached is a copy of a product brochure for the Matrox RT.X2 system for professional NLE systems which includes a card, similar to the Zahn card, that is inserted into an option card slot of a PC. Home NLE systems are also commonly available, as indicated by the attached pages describing the Turtle Beach Video Advantage PCI video production system. The point here is that the claimed invention is not a NLE system of the Zahn type.

Mr. Funaya also addressed the Zahn reference in numbered paragraph 5 bridging pages 3 and 4 of his declaration under 37 C.F.R. 1.132. Mr. Funaya notes that "Zahn is directed to non-linear video editing which, by definition, is not time-synchronous transmission over a network."

The Examiner relies on Sastry et al. for a disclosure of "an apparatus (see FIG 1, server 220/230/260; see FIG. 3, server 310; see FIG. 4,6; server 405/605) for the transmission of time-synchronous data (see FIG. 2, real time data; see col. 3, line 29–31, 48–51, 62–67) from a sender (see FIG. 2, sending/transmitting client 241–244/251–254) to a receiver (see FIG. 2, receiving client 251–254/241–244) using a network (see FIG. 2, using network 210), where in data is processed and transmitted to the sender as well as the receiver (see FIG. 2,3,4,6, server 310 process and transmitted to sending client 241–244 as well as the receiving client 251–254; see col. 3, line 32 to col. 4, line 10) . . ." What Sastry et al. actually disclose is a voice

processing allocation scheme in an IP network to which multiple clients are connected via servers, as generally shown in Figure 2. The servers have processing modules 430 having multiple Digital Signal Processors (DSPs) 431 to 439. These DSPs implement various algorithms, such as Adaptive Differential Pulse Code Modulation (ADPCM) and Conjugated Structure Algebraic Code-Excited Linear Prediction (CS-ACELP) voice compression. These are processor intensive algorithms, and the problem addressed by Sastry et al. is the switching of active data connections from one processor to another processor without significantly interfering with the transmission of voice and other data. Sastry et al. do this using a DSP resource allocation algorithm to load share the data by selectively moving an active voice call currently being processed by one DSP to another DSP having sufficiently available processing power, without interrupting the prevailing service. The liberated DSP may then be used to process a new voice call. Figure 8 illustrates the data switching between DSPs. By load sharing among the DSPs, the number of simultaneous active voice calls supported by a voice processing module may be increased.

The DSP load sharing scheme of Sastry et al. is not the same or analogous to the claimed invention. In the claimed invention, adaptation to changed data rate and/or network characteristics has to be performed without further degradations of transmission quality. This is achieved through the setup of a parallel processing unit which is adapted to the changed data rate and/or network characteristics. This is not load sharing among a plurality of identical processors, as in Sastry et al. Rather, what the claimed invention does is to setup a parallel processor in which the individual subcomponents of the parallel processor are adapted to the changed data rate and/or network conditions. Once the parallel processor is setup, that is, the subcomponents of the parallel processor are instantiated and initialized, processing and transmission of the time-synchronous data is performed by switching over to that processor by means of a switch.

Mr. Funaya discusses the rejection of claims 1 to 4 and 6 to 18 as being obvious in view of the Zahn and Sastry et al. references in numbered paragraph 7

beginning on page 4 and continuing to the top of page 6 of his declaration under 37 C.F.R. 1.132. Mr. Funaya notes again that claim 1 refers to a mechanism for the transmission of time-synchronous data, but Zahn does not transmit any data but operates on a single machine. As to claim 2, Mr. Funaya notes that this claim refers to the special case of necessity to change the parameters of the system during the transmission but that Zahn does not change the parameters the parameters of a video editing unit after setup. As to claim 3, Mr. Funaya notes that this claim refers to the idea of creating a connection to the second processing unit is only done when the setup and/or adaptation is already realized but that Zahn switches before setup since the timing problems of component setup time do not matter for video editing. Mr. Funaya notes that claims 6 to 18 refer to different variants of the core concept. Referring to the Sastry et al. patent, Mr. Funaya states "that in Sastry et al. all the processors are always active and perform processing operation in parallel" whereas "Applicants, on the other hand, disclose and claim a method whereby the second processing unit (or several units) is setup AFTER the switch command (which can't be known in advance in real time traffic and will be based on varying load conditions in the network or the clients)." Mr. Funaya goes on to say that "The claimed invention method ensures the DYNAMIC creation and deletion of processing chains, still no loss or interruption in the transmission will appear", whereas "Sastry et al. do not cover the problem of setup time at all."

Claim 1 recites

"a first processing unit composed of multiple subcomponents, each subcomponent being designed to process the time-synchronous data in a specific and different way, a plurality of said multiple subcomponents being selected from the group consisitng of a codec, a filter and an IP packetizer;

"a second processing unit parallel to the first processing unit, said second processing unit being composed of multiple subcomponents, each subcomponent being designed to process the time-synchronous data in a specific and different way, a plurality of said multiple subcomponents being selected from the group consisitng of

a codec, a filter and an IP packetizer, wherein the subcomponents of the second processing unit are setup and adapted based on changed sender data rate or network characteristics by configuring attribute parameters of the subcomponents, wherein data processing and transmission of the time-synchronous data is continued within the first processing unit during the setup and adaptation of the second processing unit; and

"a switch selecting between the first and second processing units, the processing and transmission of the time-synchronous multi-media data initially being performed by the first processing unit and, after switching by the switch, the processing and transmission of the time-synchronous multi-media data is performed using the second processing unit such that the processing and transmission of the time-synchronous multi-media data is performed within the second processing unit, the output of said switch being connected to said IP network."

Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over the Zahn International Patent Publication and the Sastry et al. patent in view of U.S. Patent No. 7,095,717 to Muniere. This rejection is again respectfully traversed for the reason that the combination of Zahn, Sastry et al. and Muniere does not teach, suggest or otherwise make obvious the claimed invention.

As discussed above, Zahn does not disclose the basic system recited in claim 1. The Zahn video processor board is for an entirely different function and is constructed and operates in a manner which is entirely different from the disclosed and claimed invention. The Sastry et al. load sharing scheme is not the same as the claimed setup of a parallel processor with subcomponents adapted for the changed data rate or network conditions. Muniere discloses a method for multiplexing two data flows on a radio communication channel and corresponding transmitter. Since Zahn is not transmitting data from a sender to a receiver, Muniere cannot be combined with Zahn to make a workable system. The two are in entirely different technical fields. Moreover, the claimed invention has nothing whatsoever to do with multiplexing two data flows. On the contrary, the claimed invention is concerned with

the transmission of one data flow only, the time-synchronous data of, for example, video frames. Clearly there is no basis in fact for the conclusion of obviousness based on Zahn in combination with Sastry et al. and Muniere.

Mr. Funaya addressed the rejection of claim 5 in numbered paragraphs 8 and 9 on page 6 of his declaration under 37 C.F.R. 1.132. Mr. Funaya first of all notes that "Muniere proposes a multiplexing method to ensure prioritized transmission of high priority data with enough remaining bandwidth for the low priority data to flow." Mr. Funaya notes that "In real time transmission of multimedia data of packet networks, the transmission quality of the channel can vary quickly and significantly over time." Mr. Funaya states that "claim 5 specifies a solid method for the identification of an appropriate switching condition" and Muniere does not specify any conditions, since there is no switch involved in the Muniere multiplexing method. Moreover, neither Zahn nor Sastry et al. refer to the same decision as given in claim 5.

It is respectfully submitted that the claims have been misinterpreted by the Examiner. To aid the Examiner in his reconsideration of the claims, the following comments are offered. In the claimed invention, Applicants achieve seamless handovers between potentially many different (arbitrary complex) processing units as a mechanism for optimizing transmission quality in packet-based networks and low-power devices (e.g.., mobile telephones). The central idea is to allow adaption between various independent instantiations of processing units, as determined by a particular operating environment. Processing units may contain arbitrary complex subcomponents (codecs, filters, packetizers, etc.) and may be available locally within a device or downloaded by standard means over a network connection. Applicants claimed invention is novel in that it supports seamless adaption between the current operating processing chain and newly instantiated chains either by feeding data simultaneously to both chains or utilizing additional processing resources for encoding within the second chain during setup.

In the claimed invention, Applicants switch the input of two or more independent processing units, where it is always guaranteed that only one of them is

processing at any given time. In addition, Applicants coordinate the control sequence of parallel processing unit operations (setup, teardown or resource sharing) in order to minimize processing power requirements and allow the installation of potentially useful processing units specific to a given operational environment.

The features which characterize the claimed invention include the following:

- A digital media processing system with arbitrary number of "processing units".
- Generally applicable to real-time IP streaming media scenarios.
- Processing units are "not specified" and may include arbitrary chains of codecs, packetizers, etc.
- Seamless switching is intended to accommodate additional processing units (e.g., downloaded).
- Processing chain components may contain quality settings (e.g., quantizer settings).
- Processing chains are instantiated into memory "on-demand" by adaptation algorithms.
- Seamless switching refers to instantiating a processing unit and activating its input.
- Seamless switching does accommodate processing chain instantiation timing.
- Processing chains are never fed data simultaneously.
- Processing chains never operate on input data simultaneously.
- Seamless switching may include teardown or timed caching of unneeded processing units.

In the current Office Action, the Examiner adds "Second set of rejection"; specifically, the Examiner rejects claims 1 to 13, 15, and 18 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,299,003 to Ochi et al. This rejection is respectfully traversed for the reason that the patent to Ochi et al. neither shows nor suggests the claimed invention.

Ochi et al. disclose a signal processing apparatus that allows a signal to pass through a transmission circuit in a positive time sequence and then, allows the signal to be transmitted through another transmission circuit having the same transmission characteristic in a reverse time sequence with respect to the positive time sequence. Also, while the transmission circuit is arranged to have a zero-phase characteristic, each segment of a continuous signal is processed throughout a period which is equal to at least two times a duration of an impulse response duration of the transmission circuit. In this way, unwanted waveform errors appearing at discontinuous regions of the signal will be eliminated.

In short, the Ochi patent is directed to entirely targets and an entirely different scenario, i.e., Ochi has nothing to do with the claims in the present application and it works entirely differently. For example, the very first lines of the Ochi summary (25-30) specifically state that their approach is intended to help reduce "unwanted waveform distortion" using a "frequency characteristic changing process" which is limited to a "small-size circuit" - i.e. digital signal processing techniques. Importantly, the Ochi approach relies upon signal processing chains which operate simultaneously on the same data using phase techniques to help detect and eliminate unwanted waveform errors. In short, Ochi approach demands simultaneous operation of the processing chains; which implies hardware devices with significant processing capabilities, memory and power. In contrast, claimed apparatus is specifically intended for resource-constrained mobile devices which have limited processing, memory and power capabilities. In this regard, the approach taken in the instant application attempts to lower the processing burden of such devices by only operating a single processing chain at any one time.

Moreover, the Ochi approach implies *a priori* determination and integrated hardware-based support of processing chain components relevant to a very specific set of waveform error conditions. In contrast, the approach taken in the present application attempts to help mobile devices overcome the fluctuations of IP network conditions by instantiating arbitrary processing components, possibly not known a

priori.

The instant invention may involve the dynamic download and instantiation of processing components such as codecs, packetizers, etc. and targets an entirely different domain - i.e. adaptation to the often dynamic transmission characteristics of IP networks.

Furthermore, the approach in the instant application specifically claims real-time operation with zero delay. In contrast, the Ochi approach is specifically *not* intended for real-time, low-delay scenarios and relies upon parallel processing components which are characterized by significant delay and intended for broadcast scenarios.

As shown in Figure 1 of Ochi et al., an input terminal 10 and a first transmission circuit 11 having a transmission characteristic G are provided. Also, a first memory circuit 12 having a storage capacity of M which is equivalent to at least more than two times the impulse response duration α of the transmission circuit 11, is provided for storing an input signal in a predetermined time sequence and transmitting the same in the reverse of the time sequence for the length M of time. A second memory circuit 13 having a storage capacity of M which is equivalent to at least more than two times the impulse response duration α of the transmission circuit 11, is arranged for storing an input signal in a given time sequence and transmitting the same in the reverse of the time sequence for the period M after a delay time ranging from α to M-α from the action of the first memory circuit 12. Elements 14 and 15 are second and third transmission circuits which have the same transmission characteristic as that of the first transmission circuit 11. A third 16 and a fourth memory circuit 17 each having an equal storage capacity M are arranged for storage of an input signal in a given time sequence and transmission of the same in the reverse of the time sequence for the period M. A switch circuit 18 is also provided for transmitting during the period M an output signal of the third memory circuit 16 from the start of an action of the first memory circuit 12 to the start of an action of the second memory circuit 13 and an output signal of the fourth memory circuit 17 from

the start of the action of the second memory circuit 13 to the start of a succeeding action of the first memory circuit 12. A timing generator circuit 20 is provided for actuating the two memory circuits 12 and 16 and the switch circuit 18 at predetermined intervals of time. Also, a delay circuit 19 is provided for delaying an output signal of the timing generator circuit 20 and supplying to the two memory circuits 13 and 17 a resultant delay signal delayed by a given time from the start of the action of the first memory circuit 12. Element 21 is an output terminal.

In operation, an input signal (e.g. an analog or digital video signal) is fed through the input terminal 10 to the first transmission circuit 11 of transmission rate G. It is assumed that the input terminal 10 receives an input signal shown in Figure 2(a), which is expressed as a series of data blocks D1F, D1S, D2F, D2S, and so on. The signal from the first transmission circuit 11 is fed to the first memory circuit 12 where it is time base inverted at each duration (equal to the period M) from t0 to t1, t2 to t4, or t4 to t6. The signal is then transferred to the second transmission circuit 14 where its particular data blocks including D1F, D2F, and D3F, which are spaced by more than the period .alpha. (of impulse response duration) from the switching point for time base inversion, can successfully be processed regardless of the effects of a switching action, as shown in Figure 2(b). The signal is then time base inverted by the third memory circuit 16 to a row of the data blocks shown in Figure 2(c).

The second memory circuit 13 starts to operate (at a time t1) later than the first memory circuit 12. The data blocks including D1S, D2S, ad D3S shown in FIG. 2(e) are processed by the third transmission circuit 15.

The switch circuit 18 selects the output of the memory circuit 16 during the periods of t0 to t1, t2 to t3, and t4 to t5 and of the memory circuit 17 during the periods of t1 to t2, t3 to t4, and t5 to t6. Accordingly, a row of the processed data blocks shown in Figure 2(h) will be released.

Figures 3(a)-3(j) illustrate the foregoing procedure using waveforms of the signal, in which Figure 3(a) is the waveform of the original input signal; Figure 3(b) is the waveform produced by the first transmission circuit 11; Figure 3(c) is the

waveform after time base inversion at unit periods of t0 to t2, t2 to t4, t4 to t6, and so on; Figure 3(d) is the waveform after one more time base inversion action; Figure 3(f) is the waveform after time base inversion at unit periods of t1 to t3, t3 to t5, t5 to t7, and so on; Figure 3(g) is the waveform produced by the transmission circuit 15; Figure 3(h) is the waveform after a further time base inversion action; Figure 3(i) is the waveform of a control signal of the switch circuit 18, and Figure 3(j) is the waveform of the signal after switching action of the switch circuit 18.

As apparent from Figures 3(a)-3(j), the waveform of Figure 3(j) contains emphasis characteristics including preshoot and overshoot peaks. Both the preshoot and overshoot peaks in the emphasis stay between the two clip levels S1 and S2 and thus, no waveform distortion will occur in the FM demodulated playback signal.

The same effect will be obtained with the first transmission circuit 11 being coupled to the output of the switch circuit 18.

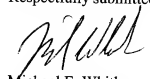
From the foregoing discussion, it will be apparent that Ochi et al. provide an entirely different signal processing apparatus for an entirely different purpose from that disclosed and claimed. The Ochi et al. apparatus does not anticipate or suggest the disclosed and claimed invention.

In view of the foregoing, it is respectfully requested that the application be reconsidered, that claims 1 to 18 be allowed, and that the application be passed to issue. In the alternative, it is requested that this amendment be entered for purposes of appeal.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

A provisional petition is hereby made for any extension of time necessary for the continued pendency during the life of this application. Please charge any fees for such provisional petition and any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,



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